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<u>L7</u>	BIOS with (protect\$4 or lock\$4 or secur\$4) with (area or location)	102	<u>L7</u>
<u>L6</u>	l4 and (programmable or FPGA)	3	<u>L6</u>
<u>L5</u>	l4 and (flash or EEPROM)	2	<u>L5</u>
<u>L4</u>	L3 and ((BIOS or (basic input output system)) with (RAM or SRAM or DRAM or (random access memory)))	3	<u>L4</u>
<u>L3</u>	l1 or l2	13	<u>L3</u>
<u>L2</u>	((6201739 or 5640349 or 6295577 or 6434695).pn.)	4	<u>L2</u>
<u>L1</u>	((5606660 or 5579522 or 5592641 or 6216224 or 5379342 or 5402383 or 6073207 or 6154838 or 6168321).pn.)	9	<u>L1</u>

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L2 prevent\$4 or lock\$4 or secur\$4)))

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L1 ((write near4 (strobe or signal or pulse)))

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Example: optical <and> (fiber <or> fibre) <in> ti
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- 4) Click Search. See [Search Examples](#)

```
(bios <sentence> (ram or
(random access memory))) and
((write <near/4> (strobe or
signal or pulse)) <paragraph>
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1 [Pen computing: a technology overview and a vision](#)

André Meyer

July 1995

ACM SIGCHI Bulletin, Volume 27 Issue 3

Full text available: [pdf\(5.14 MB\)](#)

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This work gives an overview of a new technology that is attracting growing interest in public as we visible difference from other technologies is in the use of a pen or pencil as the primary means of machine, picking up the familiar pen and paper interface metaphor. From this follows a set of cons into context with other emerging technologies and visions.Starting with a short historic ...

2 [File servers for network-based distributed systems](#)

Liba Svobodova

December 1984

ACM Computing Surveys (CSUR), Volume 16 Issue 4

Full text available: [pdf\(4.23 MB\)](#)

Additional Information: [full citation](#), [references](#), [citing](#), [index te](#)

3 [The Ada issues: A readers' guide to the Ada issues](#)

Erhard Ploedereder

May 1998

ACM SIGAda Ada Letters, Volume XVIII Issue 3

Full text available: [pdf\(2.84 MB\)](#)

Additional Information: [full citation](#)

4 [Sequential thematic organization of publications: how to achieve coherence in proposals and](#)

J. R. Tracey, D. E. Rugh, W. S. Starkey

August 1999

ACM SIGDOC Asterisk Journal of Computer Documentation, Volume 23 Issue 3

Full text available: [pdf\(3.80 MB\)](#)

Additional Information: [full citation](#), [index terms](#)

5 [Data and memory optimization techniques for embedded systems](#)

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P April 2001

ACM Transactions on Design Automation of Electronic Systems (TODAES), Vo

Full text available: [pdf\(339.91 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing](#)

We present a survey of the state-of-the-art techniques used in performing data and memory-relat

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The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or metrics: area, performance, and power dissipation of the resulting implementation. We first examine optimizations in the form of code transformations. We next cover a broad spectrum of optimizations

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, high-level synthesis, memory architecture customization, memory power dissipation, register file,

6 Concurrency, latency, or system overhead: which has the largest impact on uniprocessor D

Vinodh Cuppu, Bruce Jacob

May 2001

ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual Computer architecture, Volume 29 Issue 2

Full text available:



pdf(904.17 KB)



[Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing:](#)

Given a fixed CPU architecture and a fixed DRAM timing specification, there is still a large design space. Parameters include the number of memory channels, the bandwidth of each channel, burst sizes, turnaround overhead, memory-controller page protocol, algorithms for assigning request priorities etc. In this design space, we see a wide variation in application execution times: for example, ...

7 Is it live or is it Memorex?

Tory Sawyer, Randy Anderson, Gary McCuaig

September 1986

Proceedings of the 14th annual ACM SIGUCCS conference on User services:

Full text available:



pdf(2.60 MB)

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8 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997

Proceedings of the 1997 conference of the Centre for Advanced Studies on C

Full text available:



pdf(4.21 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index](#)

Understanding distributed applications is a tedious and difficult task. Visualizations based on process graphs obtain a better understanding of the execution of the application. The visualization tool we use is from the University of Waterloo. However, these diagrams are often very complex and do not provide the user with a good application. In our experience, such tools display repeated occurrences of non-trivial communication patterns ...

9 Cache Memories

Alan Jay Smith

September 1982

ACM Computing Surveys (CSUR), Volume 14 Issue 3

Full text available:



pdf(4.61 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

10 A coherent distributed file cache with directory write-behind

Timothy Mann, Andrew Birrell, Andy Hisgen, Charles Jerian, Garret Swart

May 1994

ACM Transactions on Computer Systems (TOCS), Volume 12 Issue 2

Full text available:



pdf(3.21 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing:](#)

Extensive caching is a key feature of the Echo distributed file system. Echo client machines maintain data and properties, with write-behind (delayed write-back) of all cached information. Echo specifies write-behind, enabling applications to store and maintain consistent data structures in the file system even if some writes from being completed. In this paper we describe ...

Keywords: coherence, file caching, write-behind

11 Energy-aware design of embedded memories: A survey of technologies, architectures, and c

Luca Benini, Alberto Macii, Massimo Poncino

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available:  pdf(288.44 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index](#)

Embedded systems are often designed under stringent energy consumption budgets, to limit heat memory systems consume a significant amount of energy to store and to forward data, it is then i consumption and performance in memory system design. Contemporary system design focuses on energy consumption in processing and storage units, as well as in their interconnections. Although

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system

12 A shared, segmented memory system for an object-oriented database

Mark F. Hornick, Stanley B. Zdonik

January 1987 **ACM Transactions on Information Systems (TOIS)**, Volume 5 Issue 1

Full text available:  pdf(2.05 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing:](#)

This paper describes the basic data model of an object-oriented database and the basic architecture particular, a secondary storage segmentation scheme and a transaction-processing scheme are discussed. It allows for arbitrary clustering of objects, including duplicates. The transaction scheme allows for more flexibility from those that enforce serializability to those that are nonserializable and require communication ...

13 Structured machine design: An ongoing experiment

Richard F. Hobson

May 1981 **Proceedings of the 8th annual symposium on Computer Architecture**

Full text available:  pdf(872.83 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing:](#)

In the following sections, the needs of structured architecture from the point of view of a single-user machine is introduced, and its design is treated as an ongoing experiment in structured machine design. Historical evidence suggests that computer architecture (hardware and software) evolves slowly, rather than through everyday use.

14 Abstract state machines capture parallel algorithms

Andreas Blass, Yuri Gurevich

October 2003 **ACM Transactions on Computational Logic (TOCL)**, Volume 4 Issue 4

Full text available:  pdf(610.28 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index](#)

We give an axiomatic description of parallel, synchronous algorithms. Our main result is that even for step, by an abstract state machine with a background that provides for multisets.

Keywords: ASM thesis, Parallel algorithm, abstract state machine, postulates for parallel computation

15 A memory management unit and cache controller for the MARS system

Feipei Lai, Chyuan-Yow Wu, Tai-Ming Parng

November 1990 **Proceedings of the 23rd annual workshop and symposium on Microprogram**


Full text available:  pdf(1.07 MB)

Additional Information: [full citation](#), [abstract](#), [references](#)

For large caches, the interaction between cache access and address translation affects the machine memory. The physically addressed caches slow down the cache access due to the virtual address translation. Virtually addressed caches is faster, but the synonym problem is difficult to handle. By some software constraints and physically addressed physically tagged caches can achieve the same speed as traditional virtually addressed

16 Parallel execution of prolog programs: a survey

Gopal Gupta, Enrico Pontelli, Khayri A.M. Ali, Mats Carlsson, Manuel V. Hermenegildo
July 2001 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume

Full text available:  pdf(1.95 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citing](#)

Since the early days of logic programming, researchers in the field realized the potential for exploiting execution of logic programs. Their high-level nature, the presence of nondeterminism, and their re characteristics, make logic programs interesting candidates for obtaining speedups through parallel that the typical applications of logic programming frequently involve irregular computatio ...

Keywords: Automatic parallelization, constraint programming, logic programming, parallelism, pr

17 Associative and Parallel Processors


Kenneth J. Thurber, Leon D. Wald
December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4

Full text available:  pdf(2.62 MB)

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18 Functional Testing of Semiconductor Random Access Memories


Magdy S. Abadir, Hassan K. Reghbati
September 1983 **ACM Computing Surveys (CSUR)**, Volume 15 Issue 3

Full text available:  pdf(1.58 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index te](#)

19 Interactive Editing Systems: Part II

Norman Meyrowitz, Andries van Dam
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available:  pdf(9.17 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index te](#)

20 The Flux OSKit: a substrate for kernel and language research

Bryan Ford, Godmar Back, Greg Benson, Jay Lepreau, Albert Lin, Olin Shivers
October 1997 **ACM SIGOPS Operating Systems Review , Proceedings of the sixteenth ACM : principles**, Volume 31 Issue 5

Full text available:  pdf(2.47 MB)

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